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HP E2434C

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2. Were you satisfied with the operation of the preprocessor interface at turn-on?	[ ]	[ ]

3. Were the proper accessories supplied with your product?

If not, what was missing?

Cables [ ] Manual(s) [ ] Other _____

4. What measurements will this preprocessor interface be used to make?

_____

5. Which logic analyzer are you using?

Type_____

6. What do you like most about the preprocessor interface? _

_____

7. What would you like to see changed or improved?_____

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HP E2434C
Intel 80C186EC/188EC
Preprocessor Interface
User's Guide

for the HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A/62A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, and HP 16550A Logic Analyzers

Manual Part Number E2434-97002 Printed in U.S.A. August 1993

Printing History

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The dates on the title page change only when a new edition is published.

A software code may be printed after the date; this indicates the version of the software product at the time the manual or update was issued. Many product updates and fixes do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one to one correspondence between product updates and manual updates.

Edition 1 August 1993 E2434-97002

List of Effective Pages

The List of Effective Pages gives the date of the current edition and of any pages changed in updates to that edition. Within the manual, any page changed since the last edition is indicated by printing the date the changes were made on the bottom of the page. If an update is incorporated when a new edition of the manual is printed, the change dates are removed from the bottom of the pages and the new edition date is listed in the Printing History and on the title page.

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Introduction

This user's guide includes information on using the HP E2434C Preprocessor Interface to do logic analysis on the 80C186EC and 80C188EC microprocessors. All mention of 80C186EC in this user's guide collectively refers to both the 80C186EC and 80C188EC microprocessors, unless specifically noted otherwise. The HP E2434C Preprocessor Interface provides a complete interface between any Intel 80C186EC target system and the following logic analyzers: HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A/62A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, or HP 16550A.

There are additional connectors on the preprocessor interface which do not have active circuitry between the microprocessor and the logic analyzer. Since they do not add skew to the signals, the preprocessor interface can be used for timing analysis as well as state analysis.

The HP E2434C configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with the 80C186EC microprocessor. It also loads the inverse assembler for obtaining displays of microprocessor data in the assembly language mnemonics of the microprocessor.

Logic Analyzers Supported

The following logic analyzers are supported by the HP E2434C Preprocessor Interface:

HP 1650A

This logic analyzer provides 1 k of memory depth with either 80 channels of 25 MHz state analysis or 80 channels of 100 MHz timing analysis. The HP 1650A Logic Analyzer requires HP 1650A system software version V1.11 or higher to operate with the HP E2434C Preprocessor Interface. If your HP 1650A software version is older than V1.11, load new HP 1650A software (V1.11 or higher) before loading the HP E2434C software.

HP 1650B, HP 1652B, HP 16510A, and HP 16510B

These logic analyzers provide 1 k of memory depth with either 80 channels of 35 MHz state analysis (25 MHz state analysis for the HP 16510A) or 80 channels of 100 MHz timing analysis.

HP 1660A/61A/62A

The HP 1660A/61A/62A Logic Analyzers provide 4 k of memory depth with 136 channels (HP 1660A), 102 channels (HP 1661A), or 68 channels (HP 1662A) of 100 MHz state analysis or 250 MHz timing analysis. These logic analyzers also support various combinations of mixed state/timing analysis.

HP 16511B

This logic analyzer combination provides 1 k of memory depth with either 160 channels of 35 MHz state analysis, or 80 channels of 35 MHz state analysis and 80 channels of 100 MHz timing analysis.

HP 16540A,D with one or two HP 16541A,D Expansion Cards

This logic analyzer combination provides 4 k of memory depth (16 k with the D version) with up to either 64 or 112 channels of 100 MHz state or timing analysis.

HP 16542A (Master Card and two expansion cards)

This logic analyzer combination provides 1 M of memory depth with 48 channels of 100 MHz state or timing analysis.

HP 16550A

This logic analyzer provides 4 k of memory depth with 102 channels per card of 100 MHz state analysis or 250 MHz timing analysis. This logic analyzer will also support various combinations of mixed state/timing analysis.

How to Use This Manual

This manual is organized into three chapters and one appendix:

- Chapter 1 explains how to install and configure the HP E2434C Preprocessor Interface to perform measurements with the supported logic analyzers.
- Chapter 2 provides reference information on the format specification and symbols configured by the HP E2434C software. It also provides information about the inverse assembler and status encoding.
- Chapter 3 contains additional reference information including the characteristics and signal mapping for the HP E2434C Preprocessor Interface.
- Appendix A contains information on troubleshooting problems or difficulties which may occur with the preprocessor interface.

1

Setting Up the HP E2434C

Introduction

This chapter explains how to install and configure the HP E2434C Preprocessor Interface to perform measurements with the supported logic analyzers.

Duplicating the Master Disk

Before you use the HP E2434C software, make a duplicate copy of the HP E2434C master disk. Then store the master disk and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the disk wears out, is damaged, or a file is accidently deleted.

To make a duplicate copy, use the Duplicate Disk operation in the disk menu of your logic analyzer. For more information, refer to the reference manual for your logic analyzer.

Logic Analyzer Software Compatibility

The HP E2434C Preprocessor Interface requires HP 16500A system and module software version V04.01 or higher. For the HP 16500B mainframe, system and module software version V01.02 or higher is required. For the HP 1660-series Logic Analyzers, software version V01.00 or higher is required. To use the enhanced inverse assembler with the HP 1660-series Logic Analyzers, software version V02.00 or higher is required. If your software version is older than those listed above, load new system and module software with the above version numbers or higher before loading the HP E2434C software.

For the HP 1650A Logic Analyzer, software version V01.11 or higher is required.

Equipment Supplied

The HP E2434C Preprocessor Interface consists of the following:

- The preprocessor interface hardware, which includes the preprocessor interface circuit card.
- The configuration files and inverse assembler software on a 3.5-inch disk.
- This user's guide.

Two adapters are available for connecting to target systems: HP E3424A (a 100-pin EIAJ QFP Rectangular Probe Adapter), to connect to rectangular EIAJ QFP target systems, and HP E3432A (a 100-pin PQFP Square Probe Adapter) to connect to square PQFP target systems. One of these adapters must be specified when you are ordering the product.

Minimum Equipment Required

The minimum equipment required for analysis of 80C186EC target systems consists of the following items:

- An HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A/62A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D (Master Card and one or two expansion cards), HP 16542A (Master Card and two expansion cards), or HP 16550A Logic Analyzer.
- The HP E2434C Preprocessor Interface and Inverse Assembler software.
- HP E3424A or HP E3432A, for connecting to the target system.

Note

The above equipment is the minimum required for three-pod state analysis. There are additional connectors on the preprocessor interface which can be used for timing analysis. The additional connectors require either the General Purpose Probes shipped with your logic analyzer, or one 100 kOhm Termination Adapter per connector (HP part number 01650-63203).
The CLKIN and OSCOUT pins are not connected to a preprocessor interface pod; these pins can be probed at the preprocessor interface PGA socket.

Installation Overview

The following procedure describes the major steps required to perform measurements with the HP E2434C Preprocessor Interface. The page numbers listed in the various steps refer you to sections in this manual that offer more detailed information.

Caution

To prevent equipment damage, be sure to remove power from both the target system and the logic analyzer whenever the preprocessor interface is being connected or disconnected.

1. Plug the logic analyzer pods into the preprocessor interface as shown in table 1-1 on page 1-8 (state) or table 1-2 on page 1-9 (timing). The 2 x 20-pin wide connectors do not require termination adapters. For pods P2, P5, P6, P7, and P8 (and the non-terminated P1 and P3 connectors), connect 100 kOhm Termination Adapters (see page 1-5), or use the General Purpose (GP) probes shipped with your logic analyzer.
2. Connect the selected probe adapter to the target system (see page 1-4; use the Operating Note included with your adapter for detailed installation instructions). Connect the preprocessor interface to the probe adapter.
3. Load the logic analyzer configuration and inverse assembler by loading the appropriate file from the disk (see page 1-10).

You are now ready to make measurements with the logic analyzer. The rest of this chapter contains more detailed information on setting up the hardware and software.

Attention!

The Attention! symbol is used to indicate areas which might easily be overlooked, causing unexpected results. The Attention! symbol is used on several places on the signal labels which mount over the preprocessor interface. For a complete description of the areas which are marked with Attention! see page 1-11.

Connecting to the Target System

The HP E2434C Preprocessor Interface requires the HP E3424A to connect to EIAJ QFP target systems, or the HP E3432A to connect to PQFP target systems. One of these adapters must be requested when ordering the preprocessor interface.

The connection options come with a detailed Operating Note, containing instructions for connecting the probe adapter to the target system and preprocessor interface. Read the instructions thoroughly before installing the probe adapter. Figure 1-1 shows the location of Pin A1.

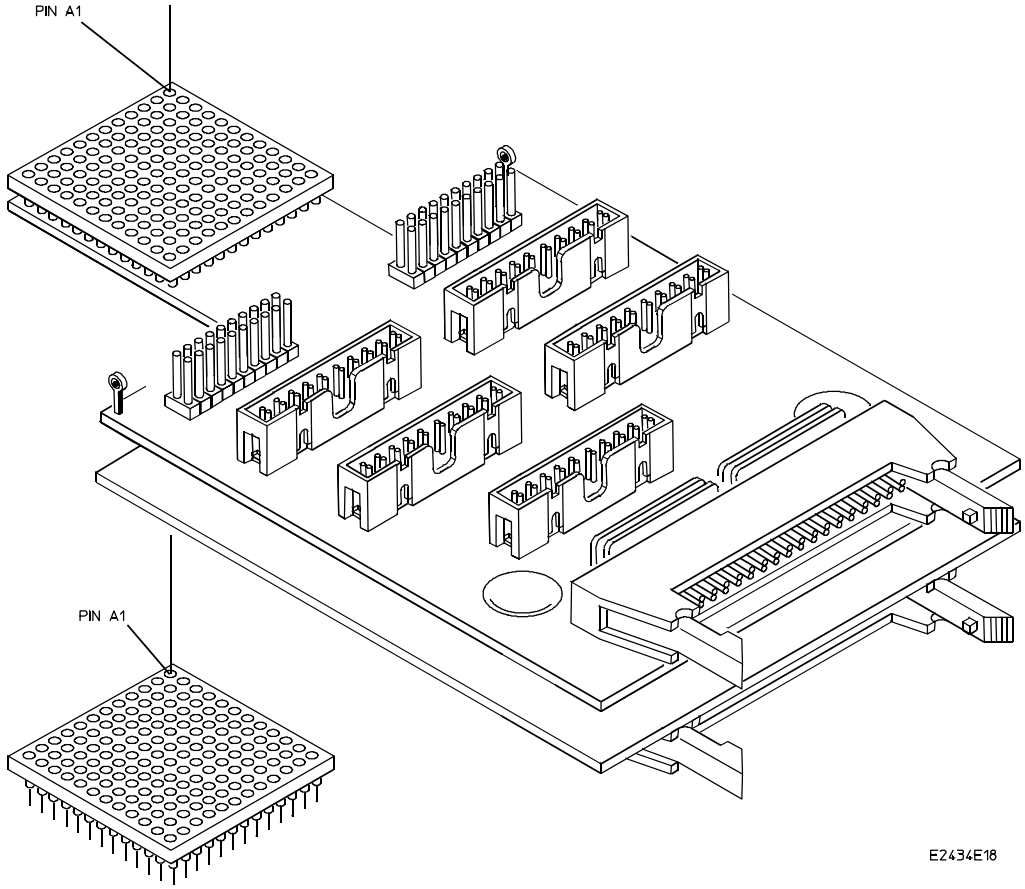

Figure 1-1. HP E2434C Preprocessor Interface

Connecting the Termination Adapters

The logic analyzer probes must be properly terminated for the logic analyzer to operate correctly. On the preprocessor interface, there are ten connectors. P4 has only a terminated connector. P1 and P3 have both terminated and nonterminated connectors, while P2, P5, P6, P7 and P8 only have nonterminated connectors. You can probe P2, P5, P6, P7 and P8 (and the nonterminated P1 and P3 connectors) with the General Purpose Probes shipped with your logic analyzer or by using 100 kOhm Termination Adapters (HP part number 01650-63203). The following steps explain how to connect the termination adapters to the preprocessor interface:

1. Align the key on the end of the termination adapter with the slot on the connector of one of the logic analyzer cables, and push the termination adapter into the connector.
2. Connect the other end of the termination adapter to the preprocessor interface (see figure 1-2).
3. Repeat steps 1 and 2 for each termination adapter.

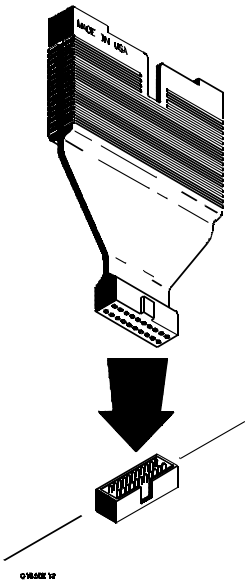

Figure 1-2. Connecting the Termination Adapter

Connecting to the HP E2434C

Connect the logic analyzer cables to the preprocessor interface as shown in the following tables. Table 1-1 is for state analysis, and table 1-2 is for timing analysis. Descriptions such as P1 refer to connectors on the preprocessor interface, while Pod 1 refers to a logic analyzer pod. Figure 1-3 shows the relative locations of the logic analyzer cards.

Note

HP 16542A with three or four Expansion Cards

The locations for the HP 16542A expansion cards, relative to the Master Card, depend on the number of expansion cards used. If one or two expansion cards are used, Card 1 is located above the Master Card and Card 2 is located below the Master Card. If three expansion cards are used, two of them are located above the Master Card and the third is located below the Master Card. When four expansion cards are used, they are located as shown in figure 1-3.

Tables 1-1 and 1-2 show the physical location and connections for a two-expansion-card system. If you are using more than two expansion cards, check the Format menu in the logic analyzer to see where the pods should be connected.

Powering the HP E2434C

Power is supplied to the HP E2434C from the logic analyzer through the P4 state connector. An additional + 5 V source is available on the P6 (Timing) pod at pin 1. For state analysis, you may need to connect to power pin on pod P6. If you do not have a Termination Adapter, you can use the short ground lead (01650-82103), and connect the logic analyzer cable + 5 pin to pin 1 of P6 (see figure 1-4, page 1-12).

Power Up / Down Sequence

When powering up, the logic analyzer must be powered up first, and then the target system. The logic analyzer provides the power to the active circuits on the preprocessor interface; unpowered circuits may cause improper operation of the target system.

When powering down, the target system should be powered down first, and then the logic analyzer.

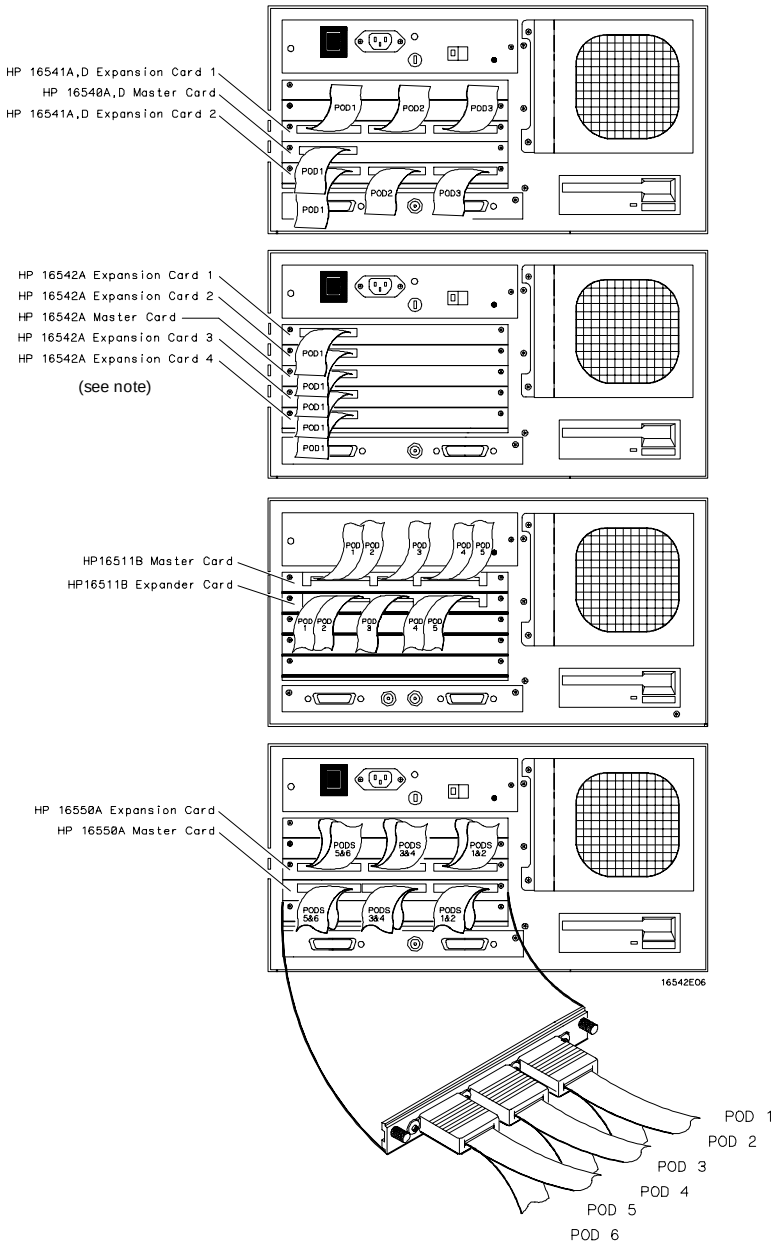

Figure 1-3. Logic Analyzer Card Locations (relative locations, actual slots used may vary)

Table 1-1. Logic Analyzer Connections and Configuration Files (State)

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 1650A, HP 1650B, HP 1652B, HP 16510A, and HP 16510B	C186EC_1		*	P4 (ADDR/ STAT)	P3 (ADDR)	** P6	P1 J↓ (DATA)
HP 16511B Upper Card	C186EC_3		--	--	--	--	--
HP 16511B Lower Card			*	P4 (ADDR/ STAT)	P3 (ADDR)	** P6	P1 J↓ (DATA)
HP 16541A,D Exp. Card 1	C186EC_5				** P6	P4 (ADDR/ STAT)	P3 (ADDR)
HP 16540A,D Master Card							P1 J↓ (DATA)
HP 16541A,D Exp. Card 2					* P5	* P7	P2 *
HP 16542A Card 1	C186EC_5						P4 (ADDR/ STAT)
HP 16542A Master Card							P1 J↓ (DATA)
HP 16542A Card 2							P3 (ADDR)
HP 1660A/61A/62A, HP 16550A	C186EC_7	*	*	P4 (ADDR/ STAT)	P3 (ADDR)	** P6	P1 J↓ (DATA)

* P2, P5, P6, P7, and P8 on the preprocessor interface are not required for inverse assembly. They can be connected to any logic analyzer pod marked with an asterisk (*), or left unconnected at the user's discretion. Use GP Probes or termination adapters to monitor these signals.

** P6 is not required for inverse assembly; it supplies additional power to power the HP E2434C (see page 1-6).

Table 1-2. Logic Analyzer Connections and Configuration Files (Timing)

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 1650A, HP 1650B, HP 1652B, HP 16510A, and HP 16510B	C186EC_2		P8	P5	P6	P7	P2
HP 16511B Upper Card	C186EC_4		--	--	--	--	--
HP 16511B Lower Card			P8	P5	P6	P7	P2
HP 16541A,D Exp. Card 1	C186EC_6				P6	P7	P2
HP 16540A,D Master Card							P5
HP 16541A,D Exp. Card 2					*	*	P8
HP 16542A Card 1	C186EC_6						P2
HP 16542A Master Card							P5
HP 16542A Card 2							P7
HP 1660A/61A/62A, HP 16550A	C186EC_8	*	P8**	P5	P6	P7	P2

* The timing configuration files are set up for pods P2, P5, P6, P7, and P8. Additional pods can be connected to any logic analyzer pod marked with an asterisk (*), or left unconnected at the user's discretion.

** For the 1660A only, connect Pod 7 of the analyzer instead of Pod 5.

Note 

The signals on P1 and P3 connectors are latched, and therefore do not provide true timing information. The P4 connector contains four signals which can be used for timing analysis; however, you can not have simultaneous state and timing measurements with P4.

Setting Up the Analyzer from the Disk

The logic analyzer is configured for state analysis by loading the appropriate configuration file. Loading this file also loads a default 16-bit inverse assembler (IA186 or IA186E, see page 2-6). To load the configuration and inverse assembler:

1. For the HP 1650A Logic Analyzer, ensure that the HP 1650A system software version is V1.11 or higher.
2. Install the HP E2434C disk in the front disk drive of the logic analyzer.
3. Select one of the following menus:
   - For the HP 1650-series logic analyzers, select the I/O Disk Operations menu;
   - For the HP 16500-series and HP 1660-series logic analyzers, select the System Front Disk menu.
4. Configure the menu to "Load" the analyzer configuration from disk.
5. For HP 16500-series and HP 1660-series logic analyzers, select the appropriate module (such as "100/500 MHz LA" or "Analyzer") for the load.
6. Use the knob to select the appropriate configuration file (see table 1-1 or 1-2).
7. Execute the load operation to load the file into the logic analyzer.

8-bit Inverse Assembler

The configuration files automatically load a default 16-bit inverse assembler. If your target system is an 80C188EC, you need the 8-bit inverse assembler. Load the configuration file from table 1-1, and then load one of the 8-bit inverse assemblers (IA188 or IA188E). To load an 8-bit inverse assembler, use steps 3 through 7 above, except that for step 6 select the inverse assembler instead of the configuration file.

If you have an 8-bit inverse assembler loaded, and store the configuration file to disk (using a different file name), you can later load the new file name, and the 8-bit inverse assembler will automatically load.

Timing Analysis

The HP E2434C can also be used for timing analysis. To configure the logic analyzer for timing analysis, ensure that the timing connections from table 1-2 are made, and load the appropriate timing configuration file from the disk. Use steps 1 through 7 on page 1-10 to load the timing configuration.

Attention! 

The Attention! symbol occurs several places on the labels. It is in reference to timing analysis, and indicates the following items which may be unexpected:

- The signals on the nonterminated (Timing) P1 and P3 connectors are latched. For true timing on the multiplexed Address/Data bus, use P2.
- The DEN signal on P1 (Timing) and P1 (State) has been routed through a delay circuit. Use P5 (Timing) to get DEN as a clock, and P7 (Timing) to get DEN as a data bit.

The Attention! symbol is also shown on the QFP probe label. Refer to the Operating Note to ensure proper connection.

Probing With an Oscilloscope

The individual pins on the preprocessor interface can also be probed with an oscilloscope. There are two ground pins on the top of the preprocessor interface (see figure 1-4). Connect the ground lead of the oscilloscope to one of the ground pins on the preprocessor interface, and the other lead to the signal to be measured. The signals are available on the PGA socket, as well as on pods P2, P5, P6, P7, and P8 (see top of figure 1-4). Table 3-1 in Chapter 3 lists the correlation between the microprocessor signals, the PGA socket, and the connectors.

CLKIN (PGA F2) and OSCOUT (PGA F3) can be probed directly off of the PGA socket.

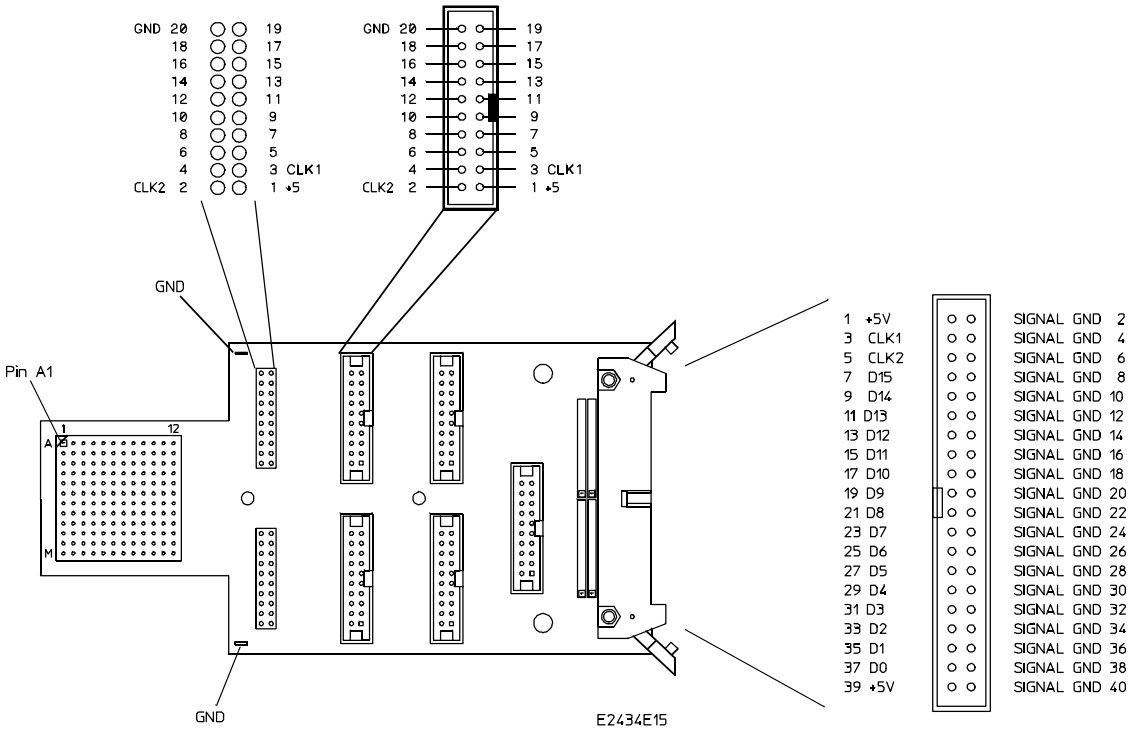

Figure 1-4. Pin Numbers and Ground Pins

2

Analyzing the Intel 80C186EC

Introduction

This chapter provides reference information on the format specifications and symbols configured by the software. It also provides information about the inverse assembler and status encoding.

State Format Specification

The 80C186EC Inverse Assembler file contains predefined format specifications, similar to that shown in figure 2-1. These format specifications include all labels for monitoring the 80C186EC microprocessor and any 80C187 coprocessors connected directly to the microprocessor.

Note

For those logic analyzers which have a Clock Period field (HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, and HP 16511B), the Clock Period field should remain in the current selection (> 60 ns) for proper HP E2434C operation. For more information on the Clock Period field, refer to your logic analyzer reference manual.

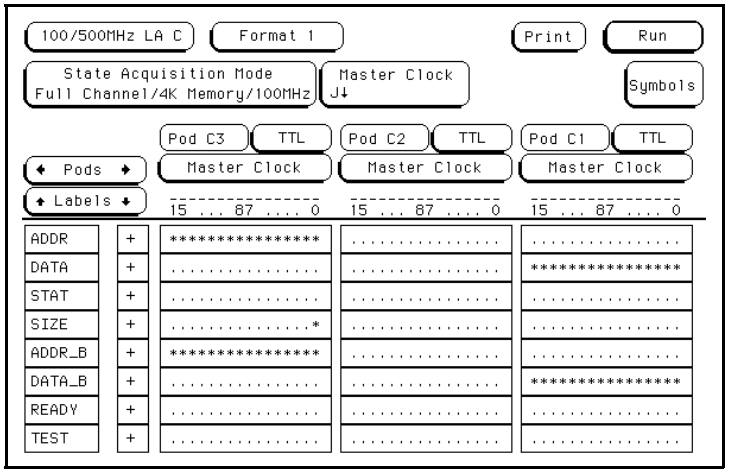

Figure 2-1. State Format Specification

Symbols

The configuration files set up symbol tables on the logic analyzer. The tables contain alphanumeric values which identify data patterns or ranges.

Table 2-1 lists the bits assigned to the STAT label. Table 2-2 lists the symbols for the STAT and SIZE labels. The patterns for each symbol listed in the tables are shown in the binary base. In the actual software, these patterns are listed in the hexadecimal base to conserve display space.

Table 2-1. STAT Label Bits

Bit	Status Signals	Description
0 - 2	$\overline{S0}$ - $\overline{S2}$	These signals indicate the type of cycle the microprocessor is executing.
3	$\overline{BHE}$	This signal indicates that data is being transferred on the most significant half of the data bus (D15 - D8).
4	S6	This signal is low for a CPU-initiated bus cycle, and high for a Refresh or DMA-initiated bus cycle.

Table 2-2. Status Field Encoding

Label	Symbol	Pattern				
		S6	**BHE**	**S2**	**S1**	**S0**
STAT	INT ACK	0	x	0	0	0
	READ IO	x	0	0	0	1
	LB READ IO	x	1	0	0	1
	WRITE IO	x	0	0	1	0
	LB WRITE IO	x	1	0	1	0
	HALT	x	x	0	1	1
	INST FETCH	0	x	1	0	0
	READ MEM	x	0	1	0	1
	LB READ MEM	x	1	1	0	1
	WRITE MEM	x	0	1	1	0
	LB WRITE MEM	x	1	1	1	0
	PASSIVE	x	x	1	1	1
			BHE	**A0**		
SIZE	HIGH BYTE XFER		0	1		
	LOW BYTE XFER		1	0		
	WORD TRANSFER		0	0		
	INVALID STATE		1	1		

Listing Menu

Captured data is displayed as shown in figure 2-2 (with the IA186 inverse assembler) or figure 2-3 (with the IA186E inverse assembler). The inverse assemblers are constructed so the mnemonic output closely resembles the actual assembly source code. In figure 2-3, the unexecuted prefetches have been suppressed.

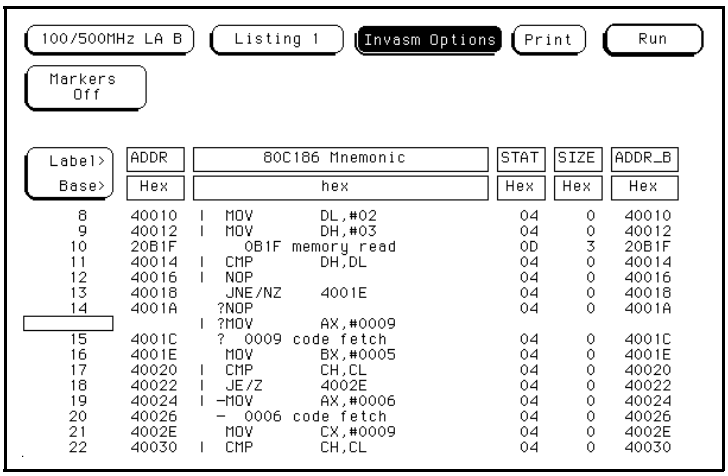

Figure 2-2. State Listing (IA186 Inverse Assembler)

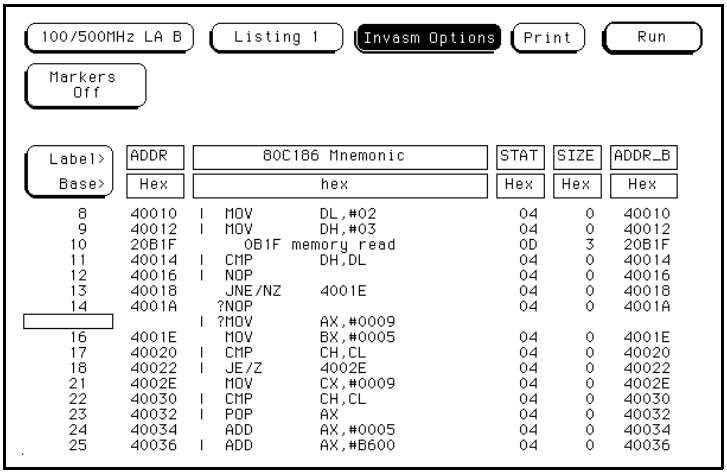

Figure 2-3. State Listing, IA186E Inverse Assembler (Unexecuted Prefetches Suppressed)

The Inverse Assemblers

The HP E2434C preprocessor Interface software contains three inverse assemblers. There are two 16-bit inverse assemblers, and one 8-bit inverse assembler. The inverse assembler with an E suffix (IA186E) is an enhanced version, which contains additional features. The enhanced inverse assembler uses the increased capabilities of the HP 16500B mainframe, or the HP 1660A/61A/62A Logic Analyzers with software version V02.00 or higher. For additional information on the IA186E features, see "The IA186E Inverse Assembler."

Synchronizing the Inverse Assembler

The microprocessor does not provide enough status information to discriminate between the first code fetch cycle of an instruction and subsequent code fetch cycles. You must point to the state that contains the first byte of an opcode fetch. Once synchronized, the inverse assembler will disassemble from this state through the end of the screen.

Use the following steps to synchronize the inverse assembler:

1. Identify a line on the display that contains the first byte of an opcode fetch.
2. Roll this line to the top of the screen.

Note 

The cursor location is not the top of the display. In figure 2-2, line 8 is at the top of the display.

3. For the IA186 inverse assembler, select the "Invasm" field at the top of the display. The listing will inverse assemble from the top line down. Any data before this screen is left unchanged.

   For the IA186E inverse assembler, select the "Invasm Options" button, and use the "Code Synchronization" portion of the submenu. With the IA186E inverse assembler, also select "Align". The listing will inverse assemble from the top line down. Any data before this screen is left unchanged.

Rolling the screen up will inverse assemble the lines as they appear on the bottom of the screen. If you jump to another area of the screen by entering a new line number, you may have to re-synchronize the inverse assembler by repeating steps 1 through 3.

Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.

Interpreting Data

Unless followed by a lower-case letter, all numeric output from the inverse assembler is in the hexadecimal format. A lower-case "o" following a numeric value indicates an octal representation (the ESC instruction for example). Decimal values are indicated by a lower-case "d" (as in the INT instruction).

Two instructions may be fetched in a single cycle because the 80C186EC can fetch a word with two instruction bytes from program memory. If the least significant byte of this word contains a single-byte instruction, the next sequential instruction begins in the upper byte. In this case, the two instructions are displayed on two separate lines on the logic analyzer display; the second instruction is prefixed by a vertical bar (|), to indicate that it begins in the upper byte.

Since instructions may begin in either the lower or upper byte, the last byte of a multiple-byte instruction may also occur in the lower byte, with a second instruction beginning in the upper byte. Thus, the following definition: Any instruction prefixed by a vertical bar begins in the upper byte of the fetched word.

Examples:

```
  PUSH DX          (PUSH occupies the lower byte;
| ADC BX,DX        ADC begins in the upper byte.)

  JO    OFLOW_CTL  (JO begins in the lower byte and uses
                    the upper byte as well. Since it is a
                    two-byte instruction, it is displayed on
                    one line.)
```

Pound signs (#) in the inverse assembler output indicate that the numbers following the pound sign (#) are immediate operands.

Asterisks (*) in the inverse assembler output indicate a portion (or portions) of an instruction was not captured by the analyzer. Missing opcodes occur frequently and are primarily due to microprocessor prefetch activity. Storage qualification, or the use of storage windows, can also lead to such occurrences.

The 80C186EC microprocessor can perform word transfers as well as byte transfers between microprocessor registers and memory. Furthermore, byte transfers may occur on either the upper eight bits or the lower eight bits of the 16-bit data bus. The inverse assembler makes a distinction between these conditions by displaying "xx" (don't care) for the byte of the transfer that was ignored by the microprocessor. In this way, it is possible to determine exactly which byte was used by the microprocessor:

28B3 memory write	(word transfer)
xxB3 memory write	(byte transfer on lower 8 bits)
28xx memory write	(byte transfer on upper 8 bits)

Prefetching Instructions in the Queue (–/?)

The 80C186EC microprocessor is a prefetching microprocessor. That is, it fetches up to three instruction words while the last opcode is still being executed. When a program executes an instruction that causes a branch, prefetched words are not used and will be discarded by the microprocessor. Unused prefetches are indicated by the prefix "–" in the inverse assembly listing.

The logic analyzer captures prefetches, even if they are not executed. Care must be taken when you are specifying a trigger condition or a storage qualification and the instruction of interest follows an instruction that may cause branching. An unused prefetch may generate an unwanted trigger.

Since the microprocessor only prefetches at most three words, one technique to avoid unwanted triggering from unused prefetches is to add "6" to the trigger address. This trigger condition will only be satisfied if the branch is not taken.

On line 18 of figure 2-2, the inverse assembler could determine that the conditional jump was taken to line 21. This was determined when the increment-by-two address sequence was broken. In this case, the inverse assembler prefixed lines 19 and 20 with "–" to indicate that these lines were not used.

In some cases, it is impossible to determine from bus activity whether or not a branch is taken or a prefetch is executed. In these cases, the inverse assembler marks the disassembled line with the prefix "?" as shown in lines 14 and 15 of figure 2-2.

Instruction Type

The 80C186EC instruction set contains four groups of instructions defining the instruction type in the second opcode byte, rather than in the first byte. In this case, if the second opcode byte is not stored in analyzer memory, only the group where an instruction resides can be determined. Therefore, the group name, rather than an instruction mnemonic, is displayed in the mnemonic display field. These group names are defined as follows:

- Immed - Contains the following instructions when used with immediate source operands:

ADD	AND
OR	SUB
ADC	XOR
SBB	CMP

- Shift - Contains the following logical and arithmetic shifts and rotates:

ROL	SHL/SAL
ROR	SHR
RCL	SAR
RCR	

- Grp_1 - Contains the following instructions:

TEST (see note)	IMUL
NOT	DIV
NEG	IDIV
MUL	

Note

The TEST instruction is included only when the instruction concerns an immediate source operand.

- Grp_2 - Contains the following groups of instructions:

INC	when the instruction concerns memory operands on 8-bit registers.
DEC	when the instruction concerns memory operands on 8-bit registers.
CALL	indirect operand.
JMP	indirect operand.
PUSH	when the instruction concerns 16-bit memory operands.

To reduce the width of the inverse assembler field, LOCK and REPeat prefixes appear on the line before the instruction to which they apply.

Abbreviations

Listed below are several abbreviations for normal programming syntax that have been adopted to reduce the width of the inverse assembler display field.

dwp	- DWORD PTR
wp	- WORD PTR
bp	- BYTE PTR
fp	- FAR PTR
np	- NEAR PTR
s	- SHORT

These symbols are displayed only if the operation size cannot be determined from the instruction itself.

Physical Addresses

Physical, rather than logical addresses, are used to perform symbolic address mapping. Most instructions, however, specify a 16-bit intrasegment offset and may indicate a segment different from the default segment for that particular instruction. Since the physical address cannot be determined from this information alone, the inverse assembler must attempt to locate the resulting bus cycle so that the physical address may be obtained. If a bus cycle of the type indicated by the initiating instruction is not found, the physical address cannot be determined and an unmapped logical address (segment override, if any, and the 16-bit intrasegment offset) is displayed instead of a mapped physical address.

Resultant bus cycles must be located in the trace list, so successful address mapping depends on the careful use of storage qualification in the logic analyzer.

Coprocessor Support

The HP E2434C Preprocessor Interface fully supports the 80C187 coprocessor. The 80C187 instructions are inverse assembled and all 80C187 operand transfers are decoded as I/O Reads and Writes.

The IA186E Inverse Assembler

The IA186E and IA188E inverse assemblers contain additional features which use the increased capabilities of some of the logic analyzers. They support the HP 16540/16541A,D and HP 16550A Logic Analyzers in the HP 16500B mainframe, and the HP 1660A/61A/62A Logic Analyzers with software version V02.00 or higher. For those logic analyzer systems, the enhanced inverse assembler is automatically loaded when the appropriate configuration file is loaded. Note that all the features in the IA186 inverse assembler are also included in the IA186E inverse assembler (see previous section).

The Inverse Assembly Options menu contains two functions: display filtering with Show/Suppress selections, and Code Synchronization (see figure 2-4). The following sections describe these functions.

Note

If the X or O pattern markers are turned on, and the designated pattern is found in a state that has been Suppressed with display filtering, the following message will appear on the logic analyzer display: "X (or O) pattern found, but state is suppressed."

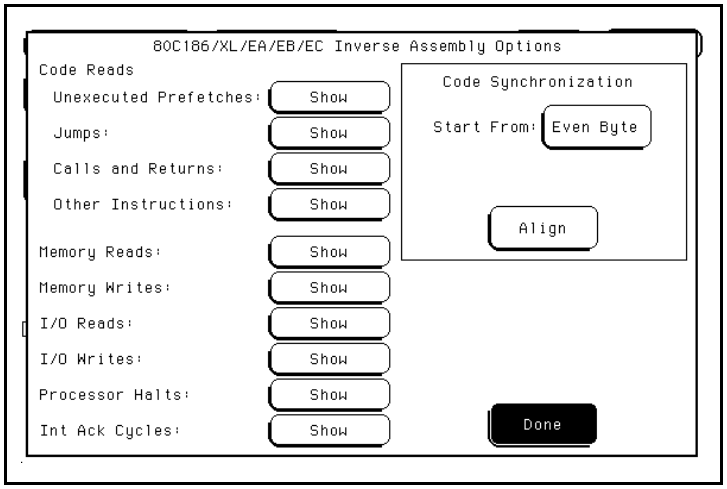

Figure 2-4. IA186E Inverse Assembly Options

Show/Suppress

The Suppress/Show settings determine whether the various microprocessor operations are shown or suppressed on the logic analyzer display. Figure 2-4 shows the microprocessor operations which have this option. The settings for the various operations do not affect the data which is stored by the logic analyzer, they only affect whether that data is displayed or not. The same data can be examined with different settings, for different analysis requirements.

This function allows faster analysis in two ways. First, unneeded information can be filtered out of the display. Figure 2-4 shows the settings to suppress unexecuted prefetches. Figure 2-3 (page 2-5) shows a listing with the unexecuted prefetches suppressed, so that only executed instructions are displayed. A comparison of figures 2-2 and 2-3 shows the difference in the listing display.

Second, particular operations can be isolated by suppressing all other operations. For example, I/O accesses can be shown, with all other operations suppressed, allowing quick analysis of I/O accesses.

Code Synchronization

The Code Synchronization enables the inverse assembler to resynchronize with the microprocessor code. In some cases the prefetch marking algorithm in the inverse assembler may lose synchronization, and unused prefetches or executed instructions may be incorrectly marked. If any of the Code Reads are suppressed, this could cause some executed instructions to be missing from the display.

To resynchronize the inverse assembler, use the procedure on page 2-6.

Timing Format Specification

When the preprocessor interface is used for timing analysis, the format specification is set up similar to that shown in figure 2-5. The formats may be slightly different, depending on which logic analyzer you are using.

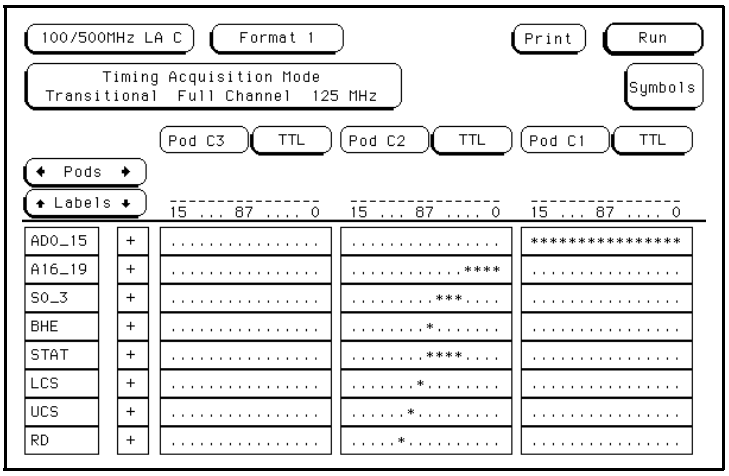

Figure 2-5. Timing Format Specification

Note

In figure 2-5 additional labels are listed offscreen. To view these signals on your logic analyzer, select the Label field and rotate the knob on the front panel clockwise.

Waveform Display

Captured timing data is displayed in the Waveform menu as shown in figure 2-6.

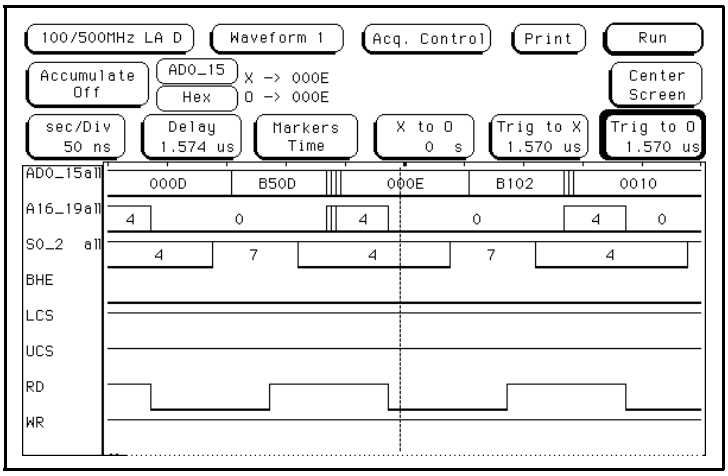

Figure 2-6. 80C186EC Waveforms Display

Note

The value to the right of the field containing AD0_15 is the pattern marked by the X marker. The base of this value is determined by the base of the specified label (AD0_15) that is specified in the timing Trace menu. The "At X (or O) marker" field allows you to select either the X or O marker. The field containing AD0_15 allows you to select any label in the Format menu.

3

General Information

Introduction

This chapter contains the characteristics and signal mapping for the HP E2434C Preprocessor Interface.

HP E2434C Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the HP E2434C Preprocessor Interface. These characteristics are included as additional information for the user.

Product Compatibility: Intel 80C186EC and 80C188EC PQFP microprocessors, Intel 80C186EC and 80C188EC EIAJ QFP microprocessors, and all microprocessors made by other manufacturers which comply with Intel 80C186EC/188EC specifications.

Microprocessor Package: 100-pin EIAJ Quad Flat Pack (QFP), S80C186EC and S80C188EC.
100-pin Plastic Quad Flat Pack (PQFP), KU80C186EC and KU80C188EC.

Clock Speed: All clock speeds up to and including 20 MHz, for all supported microprocessors.

Accessories Required: Termination Adapters or GP Probes required for timing analysis.

Signal Line Loading: Approximately 3 pF plus one "F" TTL load on AD0-15, DEN, ALE, CLKOUT, RD, and WR.
Approximately 3 pF plus one "FCT" TTL load on AD0-15, A16-19, S0-2, and BHE.
Approximately 3 pF plus two "F" TTL loads on A19/S6/ONCE.
100 kΩ plus 12 pF on all other lines.

Target Signal Timing: All Data (D0 - D15) must have 6.5 ns hold with respect to the falling edge of CLKOUT.

Logic Analyzer Required: HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A/62A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A (Master Card and two expansion cards), or HP 16550A.

Number of Probes Used:	Up to eight 16-channel probes. Three 16-channel probes are required for inverse assembly.	
Power Requirements:	1.0 A at + 5 Vdc maximum from the logic analyzer.	
Microprocessor Operations Displayed:	Memory Read/Write I/O Read/Write Instruction Fetch Interrupt Acknowledge Halt Transfer to 80C187 coprocessor	
Additional Capabilities:	The logic analyzer captures all bus cycles, including prefetches.	
Environmental Temperature:	Operating:	0 to + 55 °C (+ 32 to + 131 °F)
	Nonoperating:	–40 to + 75 °C (–40 to + 167 °F)
Altitude:	Operating:	4,600 m (15,000 ft)
	Nonoperating:	15,300 m (50,000 ft)
Humidity:	Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.	

Clocking

The logic analyzer uses the rising edge of DEN (delayed and inverted to ensure proper setup and hold for the logic analyzer) to clock information into the logic analyzer.

Interface Design

The primary function of a preprocessor interface is to connect the target microprocessor to the logic analyzer, and to perform any functions unique to that particular microprocessor. The HP E2434C Preprocessor Interface performs this primary function by latching and buffering the address, status, and data of the microprocessor so that address, status, and data can be sent to the logic analyzer at the same time.

The multiplexed Address/Data bus is demultiplexed by the preprocessor interface. The address and status latches are clocked with an inverted version of ALE. The data latches are clocked with an inverted version of the microprocessor CLKOUT.

S6 is obtained by using a delayed and logical combination of RD and WR to clock a flip-flop, with A19/S6 as the flip-flop input.

The logic analyzer uses the rising edge of DEN (delayed and inverted to ensure proper setup and hold for the logic analyzer) to clock information into the logic analyzer.

All signals can be probed on the non-terminated pods or at the PGA socket. The signals at these locations are routed straight through from the microprocessor, with no active circuitry in between. There are also four signals on P4 (terminated) which do not have active circuitry (see table 3-1). The CLKIN and OSCOUT signals can only be probed at the PGA socket on the preprocessor interface.

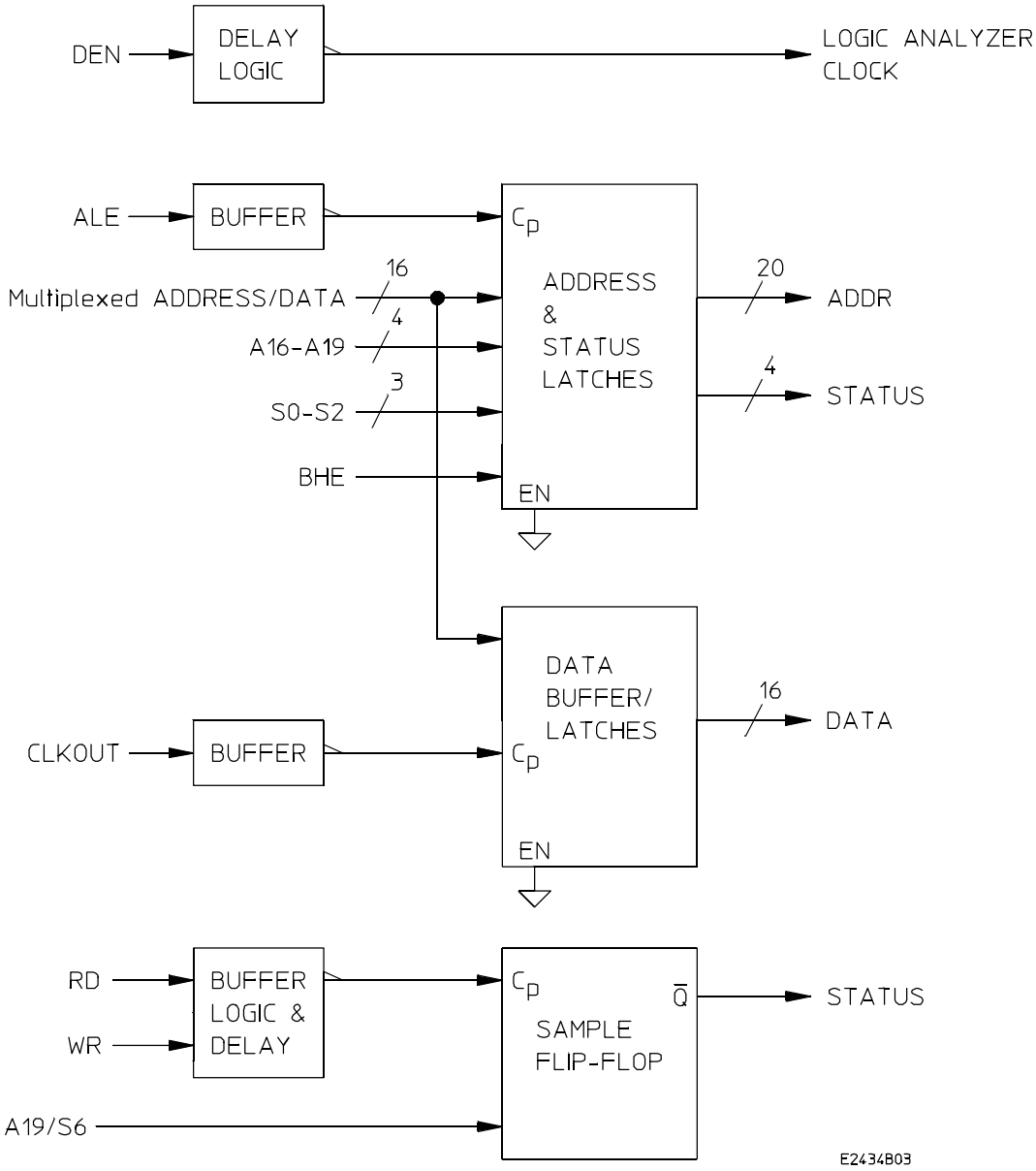

Figure 3-1. HP E2434C Block Diagram

Signal-to-Connector Mapping

The following table describes the electrical interconnections implemented with the HP E2434C Preprocessor Interface. Since the pods on the logic analyzers are numbered differently than the pods on the preprocessor interface, refer to tables 1-1 and 1-2 to correlate the pod numbers.

In table 3-1, the preprocessor interface pin numbers for pods P1 and P3 refer to the non-terminated (2 x 10) connector pins.

Table 3-1. Signal-to-Connector List

Preprocessor Pod / Pin	Logic Analyzer Bit	80C186EC QFP	80C186EC PQFP Pin	HP E2434C PGA Pin	Pin Mnemonic	Label
P3 / 19	0	76 *	73*	D12	A0	ADDR
P3 / 18	1	75 *	72*	E9	A1	ADDR
P3 / 17	2	74 *	71*	E10	A2	ADDR
P3 / 16	3	73 *	70*	E11	A3	ADDR
P3 / 15	4	69 *	66*	F11	A4	ADDR
P3 / 14	5	68 *	65*	F12	A5	ADDR
P3 / 13	6	67 *	64*	G7	A6	ADDR
P3 / 12	7	66 *	63*	G8	A7	ADDR
P3 / 11	8	63 *	60*	G11	A8	ADDR
P3 / 10	9	62 *	59*	G12	A9	ADDR
P3 / 9	10	61 *	58*	H7	A10	ADDR
P3 / 8	11	60 *	57*	H8	A11	ADDR
P3 / 7	12	59 *	56*	H9	A12	ADDR
P3 / 6	13	58 *	55*	H10	A13	ADDR
P3 / 5	14	57 *	54*	H11	A14	ADDR
P3 / 4	15	56 *	53*	H12	A15	ADDR
P7 / 19	0	80	77	C12	A16 / S3	(note 1)
P7 / 18	1	79	76	D9	A17 / S4	(note 1)
P7 / 17	2	78	75	D10	A18 / S5	(note 1)
P7 / 16	3	77	74	D11	A19/S6/ONCE	(note 1)
P7 / 15	4	81	78	A8	S0	(note 1)
P7 / 14	5	82	79	B8	S1	(note 1)
P7 / 13	6	83	80	C8	S2	(note 1)
P7 / 12	7	54	51	J11	BHE	(note 1)

* These pin numbers refer to the multiplexed Address/Data Bus. The signal on the preprocessor interface is either the latched address or the latched data information.

Note 1. These signals are not required for inverse assembly; however, they may be useful for microprocessor analysis.

Table 3-1. Signal-to-Connector List (Continued)

Preprocessor Pod / Pin	Logic Analyzer Bit	80C186EC QFP	80C186EC PQFP Pin	HP E2434C PGA Pin	Pin Mnemonic	Label
P7 / 11	8	92	89	F7	LCS	(note 1)
P7 / 10	9	91	88	E7	UCS	(note 1)
P7 / 9	10	53	50	J12	RD	(note 1)
P7 / 8	11	52	49	K11	WR	(note 1)
P7 / 7	12	55	52	J10	ALE	(note 1)
P7 / 6	13	49	46	K8	DT/R	(note 1)
P7 / 5	14	50	47	J8	DEN	(note 1)
P7 / 4	15	51	48	K12	LOCK	(note 1)
P4 / 37	0	80	77	C12	A16	ADDR
P4 / 35	1	79	76	D9	A17	ADDR
P4 / 33	2	78	75	D10	A18	ADDR
P4 / 31	3	77	74	D11	A19	ADDR
P4 / 29	4	81	78	A8	S0	STAT
P4 / 27	5	82	79	B8	S1	STAT
P4 / 25	6	83	80	C8	S2	STAT
P4 / 23	7	54	51	J11	BHE	STAT
P4 / 21	8	77	74	D11	S6	STAT
P4 / 19	9	88	85	B7	READY	(note 1, 2)
P4 / 17	10	86	83	F8	TEST	(note 1, 2)
P4 / 15	11	38	35	L6	NCS	(note 1, 2)
P4 / 13	12	12	9	F1	PDTMR	(note 1, 2)
P4 / 11	13	84	81	D8	PEREQ	(note 1, 2)
P4 / 9	14	87	84	A7	ERROR	(note 1, 2)
P4 / 7	15	39	36	K6	WDTOUT	(note 1, 2)

* These pin numbers refer to the multiplexed Address/Data Bus. The signal on the preprocessor interface is either the latched address or the latched data information.

Note 1. These signals are not required for inverse assembly; however, they may be useful for microprocessor analysis.

Note 2. These signals are not latched; they may be used for timing analysis.

Table 3-1. Signal-to-Connector List (Continued)

Preprocessor Pod / Pin	Logic Analyzer Bit	80C186EC QFP	80C186EC PQFP Pin	HP E2434C PGA Pin	Pin Mnemonic	Label
P1 / 19	0	76 *	73*	D12	D0	DATA
P1 / 18	1	75 *	72*	E9	D1	DATA
P1 / 17	2	74 *	71*	E10	D2	DATA
P1 / 16	3	73 *	70*	E11	D3	DATA
P1 / 15	4	69 *	66*	F11	D4	DATA
P1 / 14	5	68 *	65*	F12	D5	DATA
P1 / 13	6	67 *	64*	G7	D6	DATA
P1 / 12	7	66 *	63*	G8	D7	DATA
P1 / 11	8	63 *	60*	G11	D8	DATA
P1 / 10	9	62 *	59*	G12	D9	DATA
P1 / 9	10	61 *	58*	H7	D10	DATA
P1 / 8	11	60 *	57*	H8	D11	DATA
P1 / 7	12	59 *	56*	H9	D12	DATA
P1 / 6	13	58 *	55*	H10	D13	DATA
P1 / 5	14	57 *	54*	H11	D14	DATA
P1 / 4	15	56 *	53*	H12	D15	DATA
P2 / 19	0	76	73	D12	AD0	(note 1)
P2 / 18	1	75	72	E9	AD1	(note 1)
P2 / 17	2	74	71	E10	AD2	(note 1)
P2 / 16	3	73	70	E11	AD3	(note 1)
P2 / 15	4	69	66	F11	AD4	(note 1)
P2 / 14	5	68	65	F12	AD5	(note 1)
P2 / 13	6	67	64	G7	AD6	(note 1)
P2 / 12	7	66	63	G8	AD7	(note 1)

* These pin numbers refer to the multiplexed Address/Data Bus. The signal on the preprocessor interface is either the latched address or the latched data.

Note 1. These signals are not required for inverse assembly; however, they may be useful for microprocessor analysis.

Table 3-1. Signal-to-Connector List (Continued)

Preprocessor Pod / Pin	Logic Analyzer Bit	80C186EC QFP	80C186EC PQFP Pin	HP E2434C PGA Pin	Pin Mnemonic	Label
P2 / 11	8	63	60	G11	AD8	(note 1)
P2 / 10	9	62	59	G12	AD9	(note 1)
P2 / 9	10	61	58	H7	AD10	(note 1)
P2 / 8	11	60	57	H8	AD11	(note 1)
P2 / 7	12	59	56	H9	AD12	(note 1)
P2 / 6	13	58	55	H10	AD13 / CAS0	(note 1)
P2 / 5	14	57	54	H11	AD14 / CAS1	(note 1)
P2 / 4	15	56	53	H12	AD15 / CAS2	(note 1)
P5 / 19	0	100	97	D5	P1.0 / GCS0	(note 1)
P5 / 18	1	99	96	C5	P1.1 / GCS1	(note 1)
P5 / 17	2	98	95	B5	P1.2 / GCS2	(note 1)
P5 / 16	3	97	94	A5	P1.3 / GCS3	(note 1)
P5 / 15	4	96	93	D6	P1.4 / GCS4	(note 1)
P5 / 14	5	95	92	C6	P1.5 / GCS5	(note 1)
P5 / 13	6	94	91	B6	P1.6 / GCS6	(note 1)
P5 / 12	7	93	90	A6	P1.7 / GCS7	(note 1)
P5 / 11	8	19	16	G2	P2.0 / RXD0	(note 1)
P5 / 10	9	20	17	G3	P2.1 / TXD0	(note 1)
P5 / 9	10	21	18	G4	P2.2 / BCLK0	(note 1)
P5 / 8	11	22	19	H1	P2.3 / CTS0	(note 1)
P5 / 7	12	23	20	H2	P2.4 / RXD1	(note 1)
P5 / 6	13	24	21	H3	P2.5 / TXD1	(note 1)
P5 / 5	14	25	22	H4	P2.6 / BCLK1	(note 1)
P5 / 4	15	26	23	J1	P2.7 / CTS1	(note 1)

Note 1: These signals are not required for inverse assembly. However, they may be useful for microprocessor analysis.

Table 3-1. Signal-to-Connector List (Continued)

Preprocessor Pod / Pin	Logic Analyzer Bit	80C186EC QFP	80C186EC PQFP Pin	HP E2434C PGA Pin	Pin Mnemonic	Label
P6 / 19	0	1	98	C1	DRQ0	(note 1)
P6 / 18	1	2	99	C2	DRQ1	(note 1)
P6 / 17	2	3	100	D1	DRQ2	(note 1)
P6 / 16	3	4	1	D2	DRQ3	(note 1)
P6 / 15	4	11	8	E6	RESIN	(note 1)
P6 / 14	5	10	7	E5	RESOUT	(note 1)
P6 / 13	6	9	6	E4	CLKOUT	(note 1)
P6 / 12	7	86	83	F8	TEST / BUSY	(note 1)
P6 / 11	8	47	44	M8	HOLD	(note 1)
P6 / 10	9	48	45	L8	HLDA	(note 1)
P6 / 9	10	38	35	L6	NCS	(note 1)
P6 / 8	11	6	3	E1	T0IN	(note 1)
P6 / 7	12	8	5	E3	T1IN	(note 1)
P6 / 6	13	5	2	D3	T0OUT	(note 1)
P6 / 5	14	7	4	E2	T1OUT	(note 1)
P6 / 4	15	88	85	B7	READY	(note 1)
P8 / 19	0	33	30	K5	INT0	(note 1)
P8 / 18	1	34	31	J5	INT1	(note 1)
P8 / 17	2	35	32	H5	INT2	(note 1)
P8 / 16	3	36	33	G5	INT3	(note 1)
P8 / 15	4	43	40	M7	INT4	(note 1)
P8 / 14	5	44	41	L7	INT5	(note 1)
P8 / 13	6	45	42	K7	INT6	(note 1)
P8 / 12	7	46	43	J7	INT7	(note 1)

Note 1. These signals are not required for inverse assembly; however, they may be useful for microprocessor analysis.

Table 3-1. Signal-to-Connector List (Continued)

Preprocessor Pod / Pin	Logic Analyzer Bit	80C186EC QFP	80C186EC PQFP Pin	HP E2434C PGA Pin	Pin Mnemonic	Label
P8 / 11	8	85	82	E8	NMI	(note 1)
P8 / 10	9	37	34	M6	INTA	(note 1)
P8 / 9	10	27	24	J2	P3.0 / RXI1	(note 1)
P8 / 8	11	28	25	J3	P3.1 / TXI1	(note 1)
P8 / 7	12	29	26	J4	P3.2 / DMAI0	(note 1)
P8 / 6	13	30	27	K1	P3.3 / DMAI1	(note 1)
P8 / 5	14	31	28	M5	P3.4	(note 1)
P8 / 4	15	32	29	L5	P3.5	(note 1)
		13	10	F2	CLKIN	
		14	11	F3	OSCOUT	
P1 / 3	CLK1	50	47	J8	DEN *	J CLOCK
P2 / 3	CLK1	55	52	J10	ALE	
P5 / 3	CLK1	50	47	J8	DEN	
P8 / 3	CLK1	9	6	E4	CLKOUT	
P3 / 3	CLK1	--	--	--	GND	

* This is a delayed and inverted version of DEN.
Note 1. These signals are not required for inverse assembly; however, they may be useful for microprocessor analysis.

The following HP E2434C PGA pin locations are connected to ground: A1, A2, A11, A12, B1, B2, B11, B12, L1, L2, L11, L12, M1, M2, M11, and M12.

The VCC pins for the microprocessor are located on the following HP E2434C PGA pin locations: F5, F6, H6, G9, F10, E12, and C7. The preprocessor interface does not utilize the microprocessor's power; these pins are treated as no connects.

Servicing

The repair strategy for the HP E2434C is board replacement. However, table 3-2 lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales/Service Office for further information on servicing the board.

Table 3-2. Replaceable Parts

HP Part Number	Description
E2413-66504	Interface Circuit Board
E2434-66503	Personality Circuit Board
E2434-68703	Inverse Assembler Disk Pouch
E3424A	100-pin EIAJ QFP Rectangular Probe Adapter
E3432A	100-pin PQFP Square Probe Adapter
1200-1712	144-pin Pin Protector

Dimensions

Figure 3-2 lists the dimensions for the HP E2434C circuit board. The dimensions are listed in inches / millimeters.

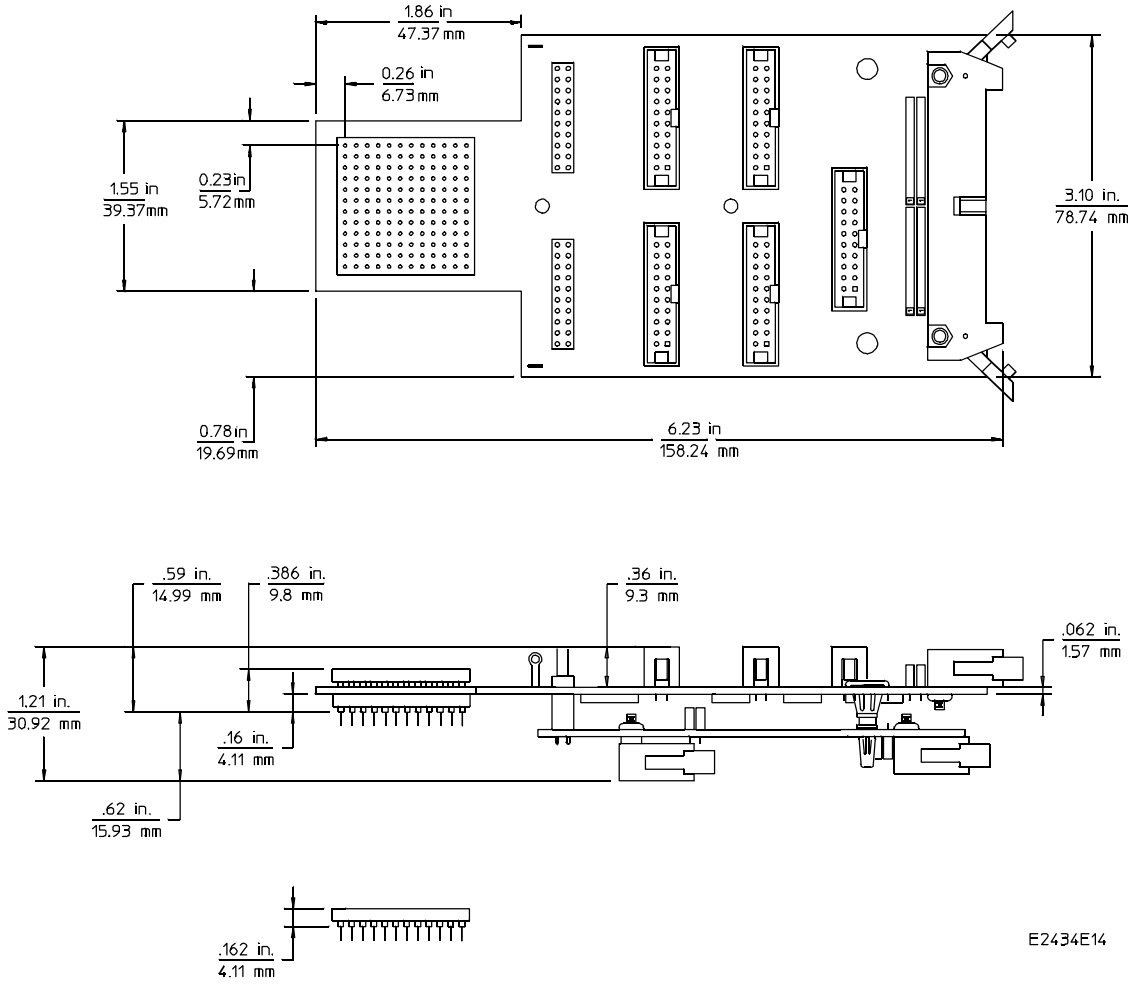

Figure 3-2. HP E2434C Dimensions – inches / mm

A

Troubleshooting

If you encounter difficulties while making measurements, use this section to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions. Error messages which may appear on the logic analyzer are listed below in quotes " ". Symptoms are listed without quotes.

If you are still having difficulties after trying the suggestions below, please contact your local Hewlett-Packard service center for additional assistance.

Target Board Will Not Bootup

If the target board will not bootup after connecting the preprocessor interface, the microprocessor or the preprocessor interface are not installed properly, or they are not making electrical contact.

- Verify that the microprocessor and the preprocessor interface are properly rotated and aligned.
- Verify that the microprocessor and the preprocessor interface are securely inserted into their respective sockets.
- Verify that the logic analyzer cables are in the proper sockets of the preprocessor interface and firmly inserted.
- Reduce the number of extender sockets (see also "Capacitive Loading").

"Slow or Missing Clock"

This error message might occur if the logic analyzer cards are not firmly seated in the HP 16500/16501A,B frame. Ensure that the cards are firmly seated.

This error might also occur if the target system is not running properly. Ensure that the target system is on and operating properly.

If the error message persists, check that the logic analyzer pods are connected to the proper connectors, as listed in table 1-1.

"No Configuration File Loaded"

Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500A/B disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.

"Selected File is Incompatible"

The logic analyzer displays this message if you try to load a configuration file for the wrong module. Ensure that you are loading an appropriate configuration file for your logic analyzer.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

No Inverse Assembly

Verify that the inverse assembler has been synchronized by placing an opcode at the top of the display and pressing the Invasm key (see "Inverse Assembler" in Chapter 2).

Incorrect Inverse Assembly

This problem is usually caused by a hardware problem in the target system. A locked status line will often cause incorrect or incomplete inverse assembly.

- Check the activity indicators for status lines locked in a high or low state.
- Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values. These labels must remain as they are configured by the configuration file.
- Verify that all microprocessor caches and memory managers have been disabled. In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly, but it may be incorrect since some of the execution trace was not visible to the logic analyzer.
- Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

No Activity on Activity Indicators

On the HP 1650A, HP 1651A, and HP 16510A Logic Analyzers, if there is no activity the fuse which allows power to the preprocessor interface is probably blown. Check the fuse in the logic analyzer. On the other logic analyzers, if there is no activity, one of the cables, board connections, or preprocessor interface connections is probably loose. Check all connections.

Capacitive Loading

Excessive capacitive loading can cause signals to degrade, resulting in incorrect capture by the preprocessor interface or system lockup in the microprocessor. All preprocessor interfaces add additional capacitive loading. The following techniques will reduce the capacitive loading:

- Remove as many pin protectors, extenders, and adapters as possible.
- If a passive preprocessor interface is available, try using that instead of an active one.

"State Clock Violates Overdrive Specification"

At least one 16-channel pod in the state analysis measurement stored a different number of states before trigger than the other pods. This is usually caused by sending a clocking signal to the state analyzer that does not meet all of the specified conditions, such as minimum period, minimum pulse width, or minimum amplitude. Poor pulse shaping could also cause this problem.

Note 

The error message "State Clock Violates Overdrive Specification" should only occur for HP 1650A,B, HP 1652B, HP 16510A,B, and HP 16511B Logic Analyzers with the Clock Period field set to < 60 ns. If this error message is observed with the Clock Period set to > 60 ns, you may have a faulty logic analyzer. If a failure is suspected in your logic analyzer, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the instrument.

Unwanted Triggers

Unwanted triggers can be caused by unexecuted prefetches. Add the prefetch queue depth to the trigger address to avoid this problem.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern did not occur. Verify that the triggering pattern is correctly set.

If a "don't care" trigger condition is set, this message indicates:

- For an HP 16511B Logic Analyzer, only one of the two cards is receiving its state clock. Refer to "Slow or Missing Clock."
- For an HP 1650A,B, HP 1652B, or HP 16510A,B Logic Analyzer, the pattern duration is probably set to less than (<) instead of greater than (>). Since a "don't care" pattern is always true, the "less than" condition is never satisfied. Set the trace menu correctly for the measurement that is desired.

Intermittent Data Errors

This problem is usually caused by incorrect signal levels. Adjust the threshold level of the data pod. Use an oscilloscope to check the signal integrity of the data lines, as needed.

Bent Pins

Bent pins on the preprocessor interface, pin protectors, or adapters can cause system errors or inverse assembly errors. Ensure all pins are properly aligned and making contact.

"Time from Arm Greater Than 41.93 ms."

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

No Setup/Hold Field on Format Screen

The HP 16540/16541A,D or HP 16542A Logic Analyzer cards are not calibrated. Refer to your logic analyzer reference manual for procedures to calibrate the cards.

"Default Calibration Factors Loaded"

The default calibration file for the logic analyzer was loaded. The logic analyzer must be calibrated when using HP 16542A or HP 16540A,D and HP 16541A,D cards. Refer to your logic analyzer manual for procedures to calibrate the master clocking system, and ensure that the "cal factors" file is saved.